



ASA-1026

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

K. WATANABE et al.

Serial No. 09/939,589

Group Art Unit: 2133

Filed: August 28, 2001

Examiner: D. Gandhi

For: SEMICONDUCTOR INTEGRATED CIRCUIT  
HAVING A SELF-TESTING FUNCTION

**TRANSMITTAL OF FORMAL DRAWINGS**

Commissioner for Patents  
Mail Stop PGPUB Drawings  
P.O. Box 1450  
Alexandria, VA 22313-1450


January 21, 2005

Sir:

Pursuant to the Notice of Allowability dated October 21, 2004, Applicants submit herewith one (1) sheet of corrected formal drawing (FIG. 4). Please substitute the enclosed sheet for the originally-filed FIG. 4 drawing.

Please charge any additional fees resulting from this action to Deposit Account No. 50-1417.

Respectfully submitted,

  
Daniel J. Stanger  
Registration No. 32,846  
Attorney for Applicants

MATTINGLY, STANGER & MALUR  
1800 Diagonal Road, Suite 370  
Alexandria, Virginia 22314  
(703) 684-1120  
Date: January 21, 2005